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(54) **Programmable digital delay unit**

Programmierbare digitale Verzögerungsschaltungseinheit

Module à retard numérique programmable

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EP-A- 0 208 049
EP-A- 0 361 806
EP-A- 0 446 891
DE-A- 4 110 340
US-A- 4 939 677
US-A- 5 204 559

EP 0 703 663 B1

Description

The present invention relates to a programmable digital delay unit, as defined in the preamble of claim 1.

As is known, a programmable digital delay unit is a unit for delaying digital data (consisting of a number of bits) for a programmable time interval, the value of which is specified by a signal.

A programmable digital delay unit is normally implemented using a RAM memory unit as shown in Figure 1 wherein the RAM memory is indicated by 1 and presents a write address selection input 2 connected to a counter 3, a read address selection input 4 connected to an adder 5, and a data input/output terminal 6. Counter 3 is supplied with clock pulses CK and in turn supplies a digital signal Z specifying the write address and which is supplied to memory 1 and adder 5. Adder 5 is also supplied with a digital delay control signal M specifying the required delay value, and supplies the memory with a digital signal M+Z specifying the read address. Memory 1 (the specific structure of which is not shown) comprises a memory cell array (with a number of cells equal to the maximum delay selectable); a write address decoder; a read address decoder; and input/output ports.

The above solution presents several drawbacks in that it involves a large number of different elements (memory cells, adders, registers, logic gates); and is limited to low-power circuits by virtue of power consumption being fixed and dependent on clock frequency. Moreover, consumption of the above known solution is difficult to reduce in that all its components must be kept on at all times for maintaining operation of the delay unit; and the maximum operating frequency of the delay unit is limited by the "fanout" of the memory address and data lines (i.e. by the maximum capacity to drive loads downstream). In fact, if the selectable delay M ranges between 0 and 2^n-1 clock strokes and is coded by an n-bit word, the address and data lines are loaded or drive 2^n memory cells. The problem may be partly solved using a dual-port RAM at the expense of an increase in cost (due to an increase in the area/transistor number ratio) and in power consumption (two address and data buses are required for simultaneously reading and writing the memory).

Another known implementation of a programmable delay unit comprises an N-1 bit slide register for delaying input data from 0 to N-1, and a multiplexer with N data inputs and an output, as shown schematically in Figure 2 wherein the slide register is indicated by 10 and is formed by a number of cascade-connected unit delay elements (flip-flops) 11. The output of each delay element 11 is therefore connected to the input of the next delay element and to one of the N inputs 13 of multiplexer 12 which also presents a selection input 14 supplied with the digital selection signal M specifying the required delay, i.e. which delay element 11 output is to be connected to its own output 15.

This solution presents the advantage of permitting a reduction in consumption when the required delay is below maximum, in which case it is possible to disable the last (N-1)-M flip-flops 11 via appropriate logic. Moreover, the fanout of each flip-flop 11 is limited to two, in that each of them only drives the next flip-flop and an input of the multiplexer, so that maximum operating frequency is higher than that of the RAM solution implemented using the same technology.

A disadvantage of the above solution, however, is that multiplexer 12 becomes increasingly difficult to implement alongside an increase in the maximum delay N-1 required, thus limiting its use to low-delay applications.

A programmable digital delay unit similar to the type defined in the preamble of claim 1 is disclosed in EP-A-0 446 891, wherein no means for reducing power consumption is provided for.

EP-A-0 361 806 discloses a variable length time delay apparatus including unit delay elements which may be selectively bypassed as defined in the preamble of claim 1.

It is an object of the present invention to provide a delay unit designed to provide for high operating frequencies, reduced consumption, a small number of similar components, and troublefree implementation.

According to the present invention, there is provided a programmable digital delay unit as claimed in Claim 1.

A number of preferred, non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figures 1 and 2 show two different known delay units;
Figures 3 to 7 show five different programmable digital delay units.

The Figure 3 delay unit, indicated as a whole by 20, comprises a number of cascade-connected delay sections 21, each of which is formed by a delay block 22, a bypass line 23, and a selector (multiplexer 24) with two data inputs, a selection input and an output. Multiplexer 24 of each delay section 21 is connected at its two data inputs to the output of the respective delay block 22 and to bypass line 23, and is supplied at its selection input with a binary selection signal S_0-S_3 specifying which of its two data inputs is to be supplied to the output. The output of multiplexer 24 of the i-th delay section 21 is connected to the input of the (i+1)-th section 21 so as to supply the latter, depending on the value of the selection signal, with the input signal or output (delayed) signal of the i-th delay section.

As shown in Figure 3, delay blocks 22 comprise a number of cascade-connected unit delay elements, e. g. flip-flops, 28. The number of unit delay elements 28 differs in each block, and more specifically decreases

to the power of two commencing from the input IN of unit 20, so that, in the example embodiment shown corresponding to a programmable delay of 0 to 15, four delay sections are provided comprising eight, four, two and one unit delay element 28 respectively as of input IN of unit 20. The first delay section therefore supplies a delay switchable from eight clock strokes to zero (8-module delay) depending on the value of the selection signal (S_3); the second delay section supplies a delay switchable from four to zero (4-module delay) depending on the value of selection signal S_2; the third delay section supplies a delay switchable from two to zero (2-module) depending on the value of S_1; and the fourth (last) delay section supplies a delay switchable from one to zero (1-module) depending on the value of S_0. Therefore, by adding the delays supplied by each section on the basis of the binary values of S_3-S_0, it is possible to obtain a delay ranging between 0 and 15.

In view of the unit delay element sequence in the successive delay sections, selection signals S_0-S_3 present a binary value equal to the corresponding bits of a four-bit digital delay signal; and as in electronic devices the programmable delay required of unit 20 is in fact specified by means of a digital word of this type, delay unit 20 requires no decoding, and the value of the individual bits constituting delay control signal M may be supplied directly to the specific multiplexers.

In the Figure 3 embodiment, unit 20 also comprises a further multiplexer 30 of the same type as 24, i.e. with two data inputs, a selection input and an output. The multiplexer 30 presents one data input connected to the input IN of unit 20 over a general bypass line 31, the other data input connected to the output of the last (fourth) delay section 21, and the selection input connected to the output of a four-input AND gate 32 supplied with the inverse of selection signals S_0-S_3 The output OUT of multiplexer 30 also constitutes the output of unit 20 so that, when no delay is required and selection signals S_0-S_3 all present a low logic value, input signal IN may be supplied directly to the output via general bypass line 31 and multiplexer 30, without going through multiplexers 24 of all the delay sections 21, thus eliminating any possibility of undesired delays.

The minimum configuration of unit 20, i.e. without multiplexer 30 and AND gate 32, comprises fifteen unit delay elements (flip-flops) 28 and four multiplexers 24. In general, a delay unit for supplying a programmable delay of 0 to 2^n-1 specified by an n-bit digital signal requires 2^n-1 flip-flops and n multiplexers. Since, as stated, the structure requires no decoding of the delay control signal, it can be implemented with a small number of only two types of components (flip-flops and multiplexers), or three types in the case of the complete solution shown in Figure 3. In view of the simple nature of the individual components involved, unit 20 is therefore easily implementable in a very small area, particularly for VLSI applications.

Another important advantage of the structure described is that it presents a maximum fanout of 2, in that each multiplexer drives only two components (the first flip-flop and the multiplexer of the next delay section) and each flip-flop drives only one component, thus permitting the use of extremely high operating frequencies.

To reduce power consumption for delays below the maximum programmable value, the Figure 3 structure is improved by providing the possibility of turning off the flip-flops of individual delay blocks 22 when bypassed by respective line 23.

Such a solution is shown in Figure 4 which is similar to Figure 3 and in which components 30-32 are omitted and unit delay elements 28 are shown in more detail in the form of D type flip-flops with a clock input 35. As shown in Figure 4, in which the components are indicated using the same numbering system as in Figure 3, the clock inputs 35 of flip-flops 28 of each delay section 21 are connected to one another and to the output of a respective two-input AND gate 36 supplied with the respective selection bit S_0-S_3 and with clock signal CK.

As such, when selection signal S_i of a specific delay section 21 presents a low logic value, by connecting the respective bypass line 23 to its output and disconnecting the output of the respective delay block, the respective AND gate 36 prevents the clock strokes from reaching the flip-flops of the delay block and in practice disables them, thus reducing consumption, on average, by half at the expense of a slight increase in complexity and area for the addition of n AND gates.

Figures 5 to 7 show further, hybrid, embodiments of the invention, wherein the potential afforded by delay blocks in decreasing numbers, as in Figures 3 and 4, is not exploited fully.

More specifically, Figure 5 shows a delay unit 40 comprising an 8-module delay section 41 (i.e. with a delay block formed by the cascade connection of eight unit delay elements 28) followed by a delay section 42 programmable from 0 to 7. Programmable delay section 42 comprises seven delay elements 28 and seven multiplexers 24, each multiplexer 24 presenting two data inputs connected respectively to the output of a preceding unit delay element 28 and to the output of the multiplexer 24 of section 41, and an output connected to the input of the next unit delay element 28. Multiplexers 24 of sections 41, 42 receive selection signals S_0-S_7 which no longer correspond to the bits of a digital delay control signal, as in the case of signal M in Figures 1-3, so that decoding logic (not shown) is required at least as regards signals S_0-S_6 (signal S_7 corresponds to the most significant bit of digital delay control signal M).

This solution presents a maximum fanout of 8 (the number of loads driven by the output multiplexer 24 of section 40) and requires 8 multiplexers.

Alternatively, embodiment 40 in Figure 5 may be modified by replacing section 41 with the cascade connection of seven 1-module sections (i.e. comprising one unit delay element 28), wherein the multiplexers 24 of each 1-module section receive at the two data inputs

the output of flip-flop 28 in its own section and the output of the multiplexer 24 of the preceding section. This provides for reducing fanout to a maximum of two and for increasing operating frequency for a given number of components.

Figure 6 shows a delay unit 44 featuring three 4-module delay sections 45 (with four unit delay elements 28) and a delay section 46 programmable from 0 to 3 and presenting three unit delay elements 28 and three multiplexers 24 connected as described with reference to Figure 5. In this case also, the multiplexers 24 of sections 45, 46 receive selection signals S_0-S_5 which no longer correspond to the bits of digital delay control signal M, so that decoding logic is required.

Delay unit 44 requires 15 unit delay elements 28 and six multiplexers 24, with a maximum fanout of four.

A different embodiment of delay unit 44 comprises the cascade connection of three 4-module delay sections 45 and three unit delay sections as described above with reference to the alternative embodiment of unit 40 in Figure 5. This solution provides for reducing fanout to a maximum of two for a given number of components and with a highly simple structure.

Figure 7 shows a delay unit 50 formed by the cascade connection of seven 2-module delay sections 51 (with two unit delay elements 28) and a 1-module delay section 52. The multiplexers 24 of sections 51, 52 receive selection signals S_0-S_7 not corresponding to the bits of delay control signal M, so that, in this case also, decoding is required.

This solution requires eight multiplexers 24, and presents a maximum fanout of two. To prevent delaying input signal IN by propagating through a large number of multiplexers when no delay is programmed, provision should be made for a general bypass line and a further multiplexer controlled by an AND gate and connected downstream from section 52 as in the Figure 3 embodiment (components 30-32).

Clearly, changes may be made to the programmable delay unit as described and illustrated herein without, however, departing from the scope of the present invention. In particular, instead of decreasing as shown, the progression of the number of delay elements in successive delay blocks may increase or present any order.

Claims

1. A programmable digital delay unit (20; 40; 44; 50) comprising a number of cascade-connected clocked delay blocks (22), each presenting an input and an output; a number of controlled bypass elements (23, 24), one for each delay block (22); each bypass element being connected to the input and to the output of the respective delay block (22) for selectively connecting said input or said output of the respective delay block to the input of the next delay block, characterized by a plurality of delay block disabling means (36), each connected to a respective delay block (22) for selectively turning off a clock signal for the respective delay block when the input of said respective delay block is connected to the input of the next delay block.

2. A delay unit as claimed in Claim 1, characterized in that at least some of said delay blocks (22) comprise a number of cascade-connected unit delay elements (28).

3. A delay unit as claimed in Claim 2, characterized in that said delay blocks (22) each comprise a number of unit delay elements (28) corresponding to powers of two.

4. A delay unit as claimed in Claim 3, characterized in that the number of unit delay elements (28) of delay blocks (22) connected downstream to one another is equal to powers of two in arithmetical progression.

5. A delay unit as claimed in Claim 3, characterized in that the number of unit delay elements (28) of delay blocks (22) connected downstream to one another is equal to decreasing powers of two (one, two, four, eight ...).

6. A delay unit as claimed in any one of the foregoing Claims from 1 to 5, characterized in that each said bypass element comprises a bypass line (23) and a controlled switching element (24); each said bypass line (23) being connected to the input of a respective delay block (22); and each switching element (24) presenting two inputs connected respectively to the output of the respective delay block and to the respective bypass line, and an output connected to the input of the next delay block.

7. A delay unit as claimed in Claim 6, characterized in that said controlled switching element comprises a multiplexer (24) with two data inputs and a selection input.

8. A delay unit as claimed in Claim 7, characterized in that said selection inputs of said multiplexers (24) receive selection signals (S_0-S_3) together directly forming a digital delay control signal (M).

9. A delay unit as claimed in any one of the foregoing Claims from 6 to 8 and presenting an input (IN) and an output (OUT); characterized in that it comprises general bypass means (30-32) connected between said input and said output of said delay unit (20).

10. A delay unit as claimed in Claim 9, characterized in that said general bypass means comprise a two-data-input switch (30) having a first data input con-

nected to said input (IN) of said delay unit (20), a second data input connected to the output of said number of cascade-connected delay blocks (22), and a selection input connected to the output of a logic gate (32) supplied with selection signals (S_0-S_3) of said controlled switching elements (24).

11. A delay unit as claimed in any of Claims 6 to 10, wherein said switching elements (24) each present a selection input supplied with a selection signal, and said delay blocks (22) each present a clock input; characterized in that said delay block disabling means (36) comprise logic gates (36) supplied with said selection signals (S_0-S_3) for said switching elements (24) and a clock signal (CK), and in turn generating enabling signals supplied to said clock inputs of said delay blocks (22).

12. A delay unit as claimed in any of claims 2-5, characterized in that said unit delay elements are flipflops (28).

Patentansprüche

1. Eine programmierbare, digitale Verzögerungsschalteinheit (20; 40; 44; 50), die umfaßt eine Anzahl von hintereinander verbundenen, getakteten Verzögerungsblöcken (22), von denen jeder einen Eingang und einen Ausgang aufweist; eine Anzahl von gesteuerten Umgehungselementen (23, 24), eines für jeden Verzögerungsblock (22); wobei jedes Umgehungselement mit dem Eingang und dem Ausgang des entsprechenden Verzögerungsblocks (22) verbunden ist, um selektiv den genannten Eingang oder den genannten Ausgang des entsprechenden Verzögerungsblocks mit dem Eingang des nächsten Verzögerungsblock zu verbinden, **gekennzeichnet** durch eine Mehrzahl von Verzögerungsblocksperreinrichtungen (36), von denen jede mit einem entsprechenden Verzögerungsblock (22) zum selektiven Abschalten eines Taktsignals für den entsprechenden Verzögerungsblock verbunden ist, wenn der Eingang des genannten entsprechenden Verzögerungsblocks mit dem Eingang des nächsten Verzögerungsblocks verbunden ist.

2. Eine Verzögerungsschalteinheit, wie in Anspruch 1 beansprucht, **dadurch gekennzeichnet**, daß wenigstens einige der genannten Verzögerungsblökke (22) eine Anzahl von hintereinander verbundenen, einheitlichen Verzögerungselementen (28) umfaßt.

3. Eine Verzögerungsschalteinheit, wie in Anspruch 2 beansprucht, **dadurch gekennzeichnet,** daß die genannten Verzögerungsblöcke (22) jeweils eine Anzahl von einheitlichen Verzögerungselementen (28) entsprechend der Potenz von zwei umfassen.

4. Eine Verzögerungsschalteinheit, wie in Anspruch 3 beansprucht, **dadurch gekennzeichnet,** daß die Anzahl der einheitlichen Verzögerungselemente (28) der Verzögerungsblöcke (22), die stromabwärts miteinander verbunden sind, gleich der Potenz von zwei in arithmetischer Reihe sind.

5. Eine Verzögerungsschalteinheit, wie in Anspruch 3 beansprucht, **dadurch gekennzeichnet**, daß die Anzahl der einheitlichen Verzögerungselemente (28) der Verzögerungsblöcke (22), die stromabwärts miteinander verbunden sind, gleich der abnehmenden Potenz von zwei (eins, zwei, vier, acht ...) sind.

6. Eine Verzögerungsschalteinheit, wie in irgendeinem der vorhergehenden Ansprüche 1 bis 5 beansprucht, **dadurch gekennzeichnet,** daß jedes genannte Umgehungselement eine Umgehungsleitung (23) und ein gesteuertes Schalterelement (24) umfaßt; wobei jede genannte Umgehungsleitung (23) mit dem Eingang eines entsprechenden Verzögerungsblocks (22) verbunden ist; und jedes Schalterelement (24) zwei Eingänge aufweist, die jeweils mit dem Ausgang des entsprechenden Verzögerungsblocks und der entsprechenden Umgehungsleitung verbunden sind, und wobei ein Ausgang mit dem Eingang des nächsten verzögerungsblocks verbunden ist.

7. Eine Verzögerungsschalteinheit, wie in Anspruch 6 beansprucht, **dadurch gekennzeichnet,** daß das gesteuerte Schalterelement einen Multiplexer (24) mit zwei Dateneingängen und einem Auswähleingang umfaßt.

8. Eine Verzögerungsschalteinheit, wie in Anspruch 7 beansprucht, **dadurch gekennzeichnet**, daß die genannten Auswähleingänge der genannten Multiplexer (24) Auswählsignale (S_0-S_3) erhalten, die zusammen unmittelbar ein digitales Verzögerungssteuersignal (M) bilden.

9. Eine Verzögerungsschalteinheit, wie in irgendeinem der vorhergehenden Ansprüche 6 bis 8 beansprucht und die einen Eingang (EIN) und einen Ausgang (AUS) aufweist, **dadurch gekennzeichnet**, daß sie allgemeine Umgehungseinrichtungen (30-32) umfaßt, die zwischen den genannten Eingang und dem genannten Ausgang dem genannten Verzögerungsschalteinheit (20) verbunden sind.

10. Eine Verzögerungsschalteinheit, wie in Anspruch 9 beansprucht, **dadurch gekennzeichnet,** daß die genannten allgemeinen Umgehungseinrichtungen einen Schalter (30) mit zwei Dateneingängen um-

fassen, der einen ersten mit dem genannten Eingang (EIN) der genannten Verzögerungsschalteinheit (20) verbundenen Eingang hat, einen zweiten Dateneingang, der mit dem Ausgang der genannten Anzahl von hintereinander verbundenen Verzögerungsblöcken (22) verbunden ist, und einen Auswähleingang, der mit dem Ausgang eines logischen Gatters (32) verbunden ist, dem Auswählsignale (S_0-S_3) der genannten gesteuerten Schalterelemente (24) zugeführt werden.

11. Eine Verzögerungsschalteinheit, wie in irgendeinem der Anspruche 6 bis 10 beansprucht, worin die genannten Schalterelemente (24) jeweils einen Auswähleingang aufweisen, dem ein Auswählsignal zugeführt wird, und die genannten Verzögerungsblöcke (22) jeweils einen Takteingang aufweisen, **dadurch gekennzeichnet**, daß die genannten Verzögerungsblocksperreinrichtungen (36) logische Gatter (36) umfassen, denen die genannten Auswählsignale (S_0-S_3) für die genannten Schalterelemente (24) und ein Taktsignal (CK) zugeführt werden, und die wiederum Freigabesignale erzeugen, die den genannten Takteingängen der genannten verzögerungsblöcke (22) zugeführt werden.

12. Eine Verzögerungsschalteinheit, wie in irgendeinem der Ansprüche 2-5 beansprucht, **dadurch gekennzeichnet,** daß die genannten einheitlichen Verzögerungselemente Flip-Flops (28) sind.

Revendications

1. Unité à retard numérique programmable (20; 40; 44; 50) comprenant un certain nombre de blocs à retard synchronisés, connectés en cascade (22), chacun présentant une entrée et une sortie; un certain nombre d'éléments de dérivation commandés (23, 24), un pour chaque bloc à retard (22); chaque élément de dérivation étant connecté à l'entrée et à la sortie du bloc à retard respectif (22) afin de connecter de manière sélective ladite entrée ou ladite sortie du bloc à retard respectif à l'entrée du bloc à retard suivant, caractérisée par une pluralité de moyens de désactivation de blocs à retard (36), chacun étant connecté à un bloc à retard respectif (22) afin de désactiver de manière sélective un signal d'horloge du bloc à retard respectif lorsque l'entrée dudit bloc à retard respectif est connectée à l'entrée du bloc à retard suivant.

2. Unité à retard selon la revendication 1, caractérisée en ce qu'au moins certains desdits blocs à retard (22) comprennent un certain nombre d'éléments à retard unitaires connectés en cascade (28).

3. Unité à retard selon la revendication 2, caractérisée en ce que lesdits blocs à retard (22) comprennent chacun un nombre d'éléments à retard unitaires (28) correspondant à des puissances de deux.

4. Unité à retard selon la revendication 3, caractérisée en ce que le nombre d'éléments à retard unitaires (28) des blocs à retard (22) connectés en aval l'un de l'autre est égal aux puissances de deux suivant une progression arithmétique.

5. Unité à retard selon la revendication 3, caractérisée en ce que le nombre d'éléments à retard unitaires (28) des blocs à retard (22) connectés en aval l'un de l'autre est égal aux puissances décroissantes de deux (un, deux, quatre, huit,...).

6. Unité à retard selon l'une quelconque des revendications 1 à 5 précédentes, caractérisée en ce que chacun desdits éléments de dérivation comprend une ligne de dérivation (23) et un élément de commutation commandé (24); chacune desdites lignes de dérivation (23) étant connectée à l'entrée d'un bloc à retard respectif (22); et chaque élément de commutation (24) présentant deux entrées connectées respectivement à la sortie du bloc à retard respectif et à la ligne de dérivation respective, et une sortie connectée à l'entrée du bloc à retard suivant.

7. Unité à retard selon la revendication 6, caractérisée en ce que ledit élément de commutation commandé comprend un multiplexeur (24) avec deux entrées de données et une entrée de sélection.

8. Unité à retard selon la revendication 7, caractérisée en ce que lesdites entrées de sélection desdits multiplexeurs (24) reçoivent des signaux de sélection (S_0 à S_3) formant directement ensemble un signal numérique de commande de retard (M).

9. Unité à retard selon l'une quelconque des revendications 6 à 8 précédentes et présentant une entrée (IN) et une sortie (OUT); caractérisée en ce qu'elle comprend des moyens de dérivation totale (30 à 32) connectés entre ladite entrée et ladite sortie de ladite unité à retard (20).

10. Unité à retard selon la revendication 9, caractérisée en ce que ledit moyen de dérivation totale comprend un commutateur à deux entrées de données (30) présentant une première entrée de données connectée à ladite entrée (IN) de ladite unité à retard (20), une seconde entrée de données connectée à la sortie dudit certain nombre de blocs à retard connectés en cascade (22), et une entrée de sélection connectée à la sortie d'une porte logique (32) recevant les signaux de sélection (S_0 à S_3) desdits éléments de commutation commandés (24).

11. Unité à retard selon l'une quelconque des revendications 6 à 10, dans laquelle lesdits éléments de commutation (24) présentent chacun une entrée de sélection sur laquelle est délivré un signal de sélection, et lesdits blocs à retard (22) présentent chacun une entrée d'horloge; caractérisée en ce que ledit moyen de désactivation de bloc à retard (36) comprend des portes logiques (36) recevant lesdits signaux de sélection (S_0 à S_3) destinés auxdits éléments de commutation (24) et un signal d'horloge (CK), et produisant à leur tour des signaux de validation délivrés sur lesdites entrées d'horloge desdits blocs à retard (22).

12. Unité à retard selon l'une quelconque des revendications 2 à 5, caractérisée en ce que lesdits éléments à retard unitaires sont des bascules bistables (28).

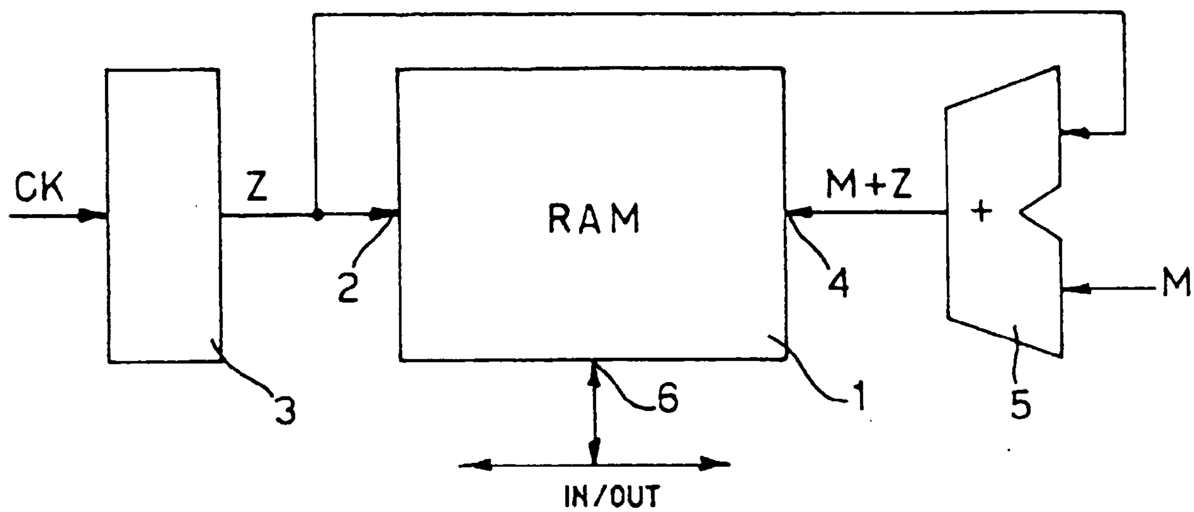
CK
Z
RAM
M+Z
+
M
2
4
3
6
1
5
IN/OUT

Fig. 1

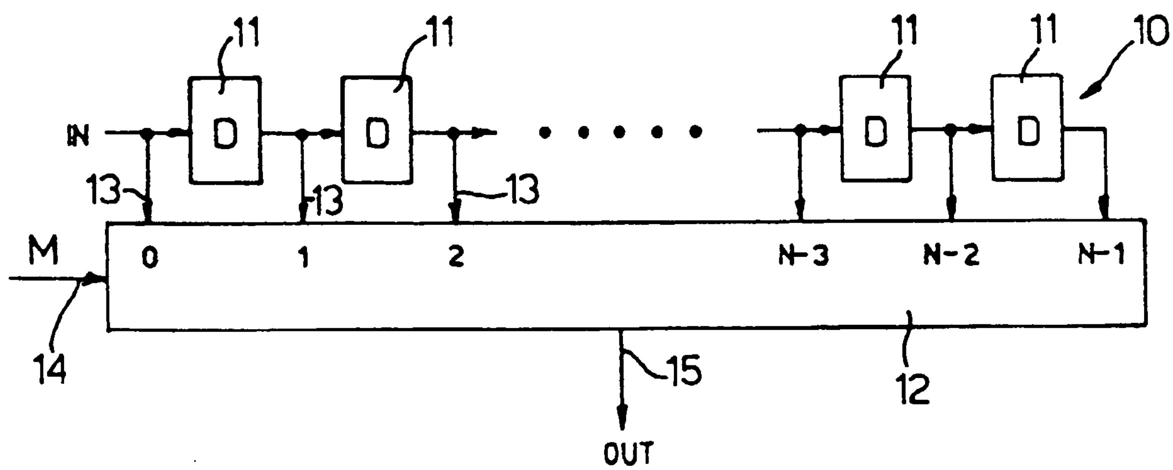
11
11
11
11
10
IN
D
D
D
D
13
13
13
M
0
1
2
N-3
N-2
N-1
14
15
12
OUT

Fig. 2

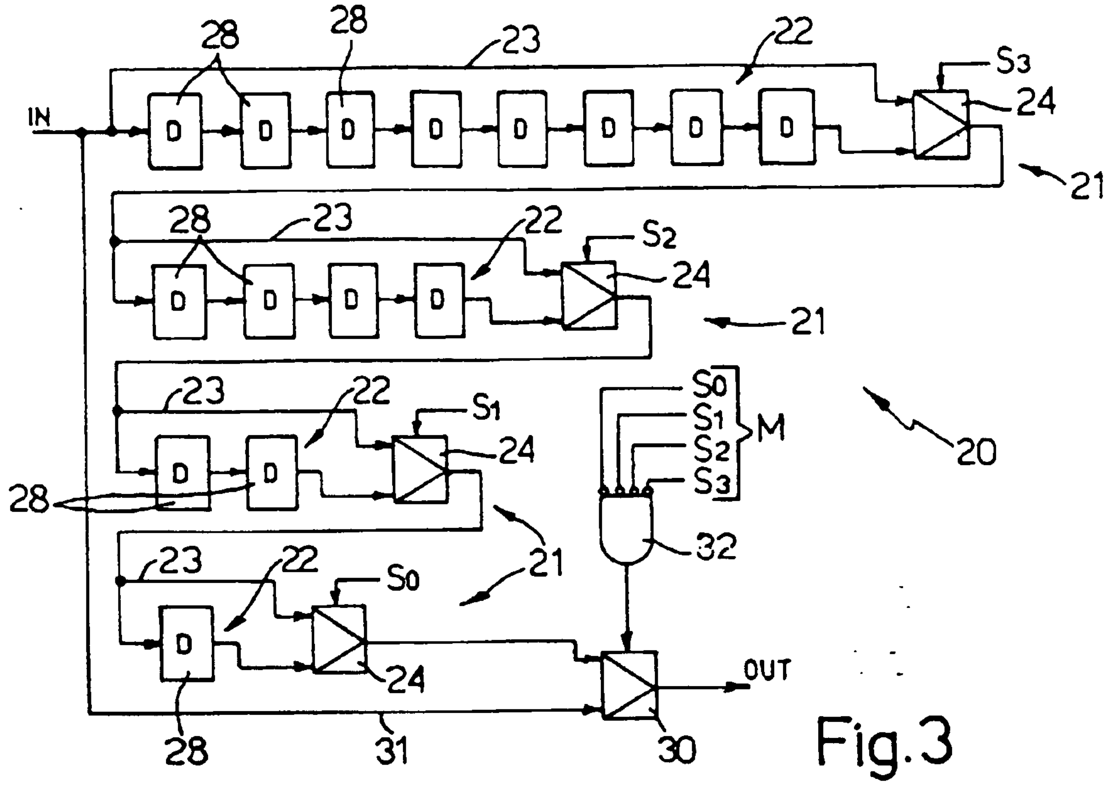
IN
D
28
23
22
S3
24
21
S2
S1
S0
M
20
32
OUT
30
31

Fig.3

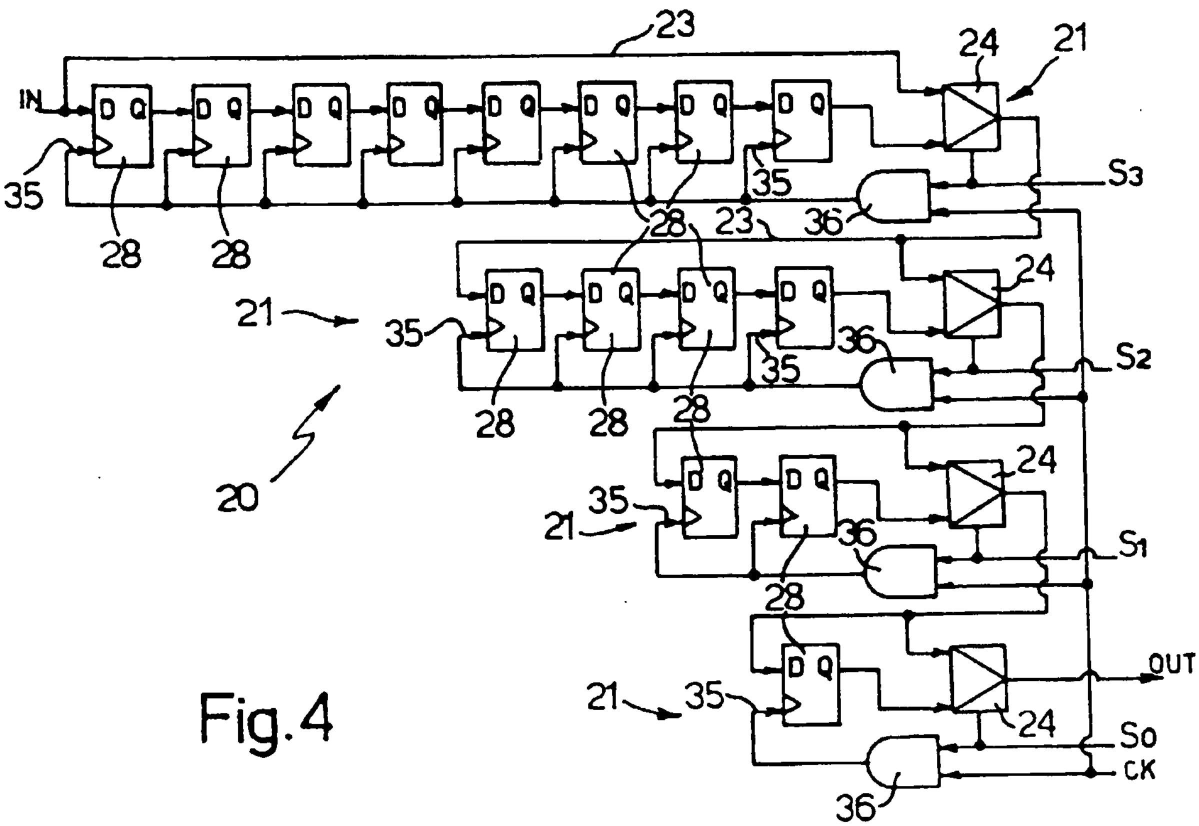
IN
D Q
23
24
21
35
28
36
S3
S2
S1
S0
CK
OUT
20

Fig.4

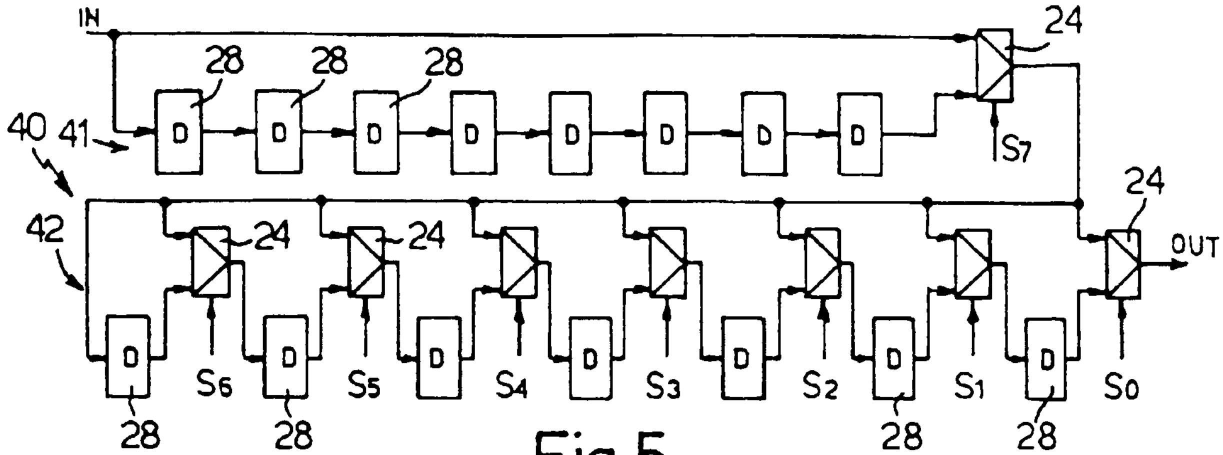

Fig.5

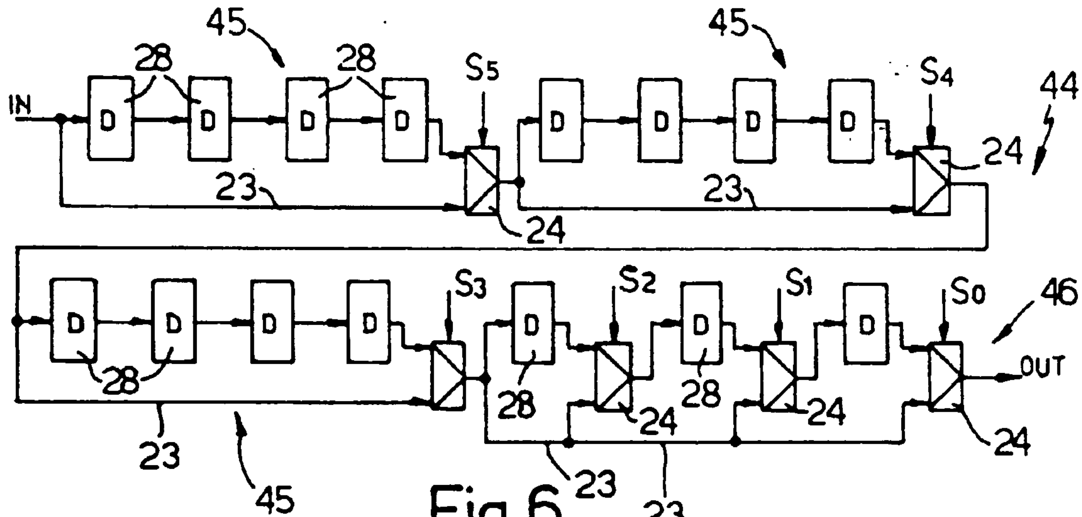

Fig.6

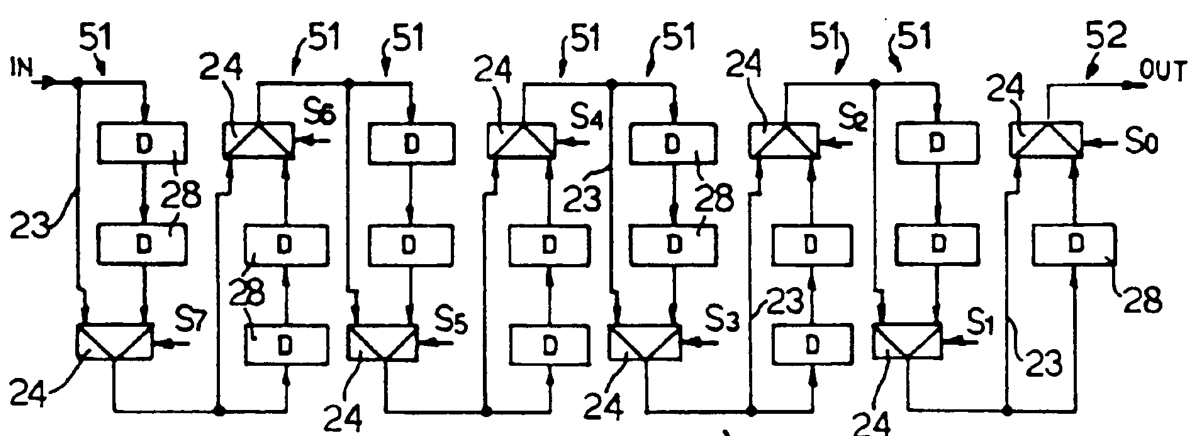

Fig.7